Abstract of the Disclosure

In a semiconductor integrated circuit, the internal clock that is synchronized to the external clock is counted to output data according to desired specification of the integrated circuit and clock counting in high frequency operation is made be possible by using parallel internal clocks having various delay times. Particularly, reduction of margin of the clock count due to error between the delay time in the delaying circuit and the time to be compensated can be prevented by independently counting the internal clock and the inverted internal clock. The semiconductor integrated circuit for generating an output control signal for controlling output of stored data includes an output control signal generating unit for delaying in parallel, by using a read command internal signal, an internal clock corresponding to an external clock received from external and the inverted internal clock, respectively, and counting the internal clock and the inverted internal clock with delay times different from each other, to output an output control signal.